Amendments to the Specification:

Please amend the specification as follows:

Please replace the title of the invention with "A MOSFET WITH A THIN GATE INSULATING FILM".

On page 1, before the heading (BACKGROUND OF THE INVENTION) insert the following:

CORRESPONDING RELATED APPLICATIONS

This application is a continuation of Application Serial No. 10/160,036 filed June 4, 2002, which is a continuation of Application Serial No. 09/828,205 filed on April 9, 2001; which is a continuation of 09/440,938 filed November 6, 1999; which in turn is a continuation of 08/527,562 filed September 13, 1995.

Please replace the first full paragraph on page 2 with the following rewritten paragraph:

To overcome this problem, in 1993, Fiegna et al. have proposed such a technique that although the gate insulating film thickness is fixed to about 3 nm, the composing elements other than the gate insulating film can be reduced [[[]](as reported by Document (Writer): C. Fiegna. H. Iwai, T. Wada, T. Saito, E. Sangiorgio, and B. Ricco; (Title) a new scaling methodology for the 0.1 to 0.021 um MOSFET, 'Dig. of Tech. Papers, VLSI Symp; (Source) Technol., Kyoto, pp. 33-34, 1993). On the basis of this technique, in the same year, Ono et al. have realized a translator having a gate length of 0.04 um, [as reported by Document (Writer): M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, and H. Iwai; (Title) Sub-50 nm gate length n-MOSFETs with 10 nm phosphorus source and drain junction: (Source) IEDM Tech. Dig., pp. 119 to 122, 1993)][[]]].

Please replace the second full paragraph on page 7 with the following rewritten paragraph: